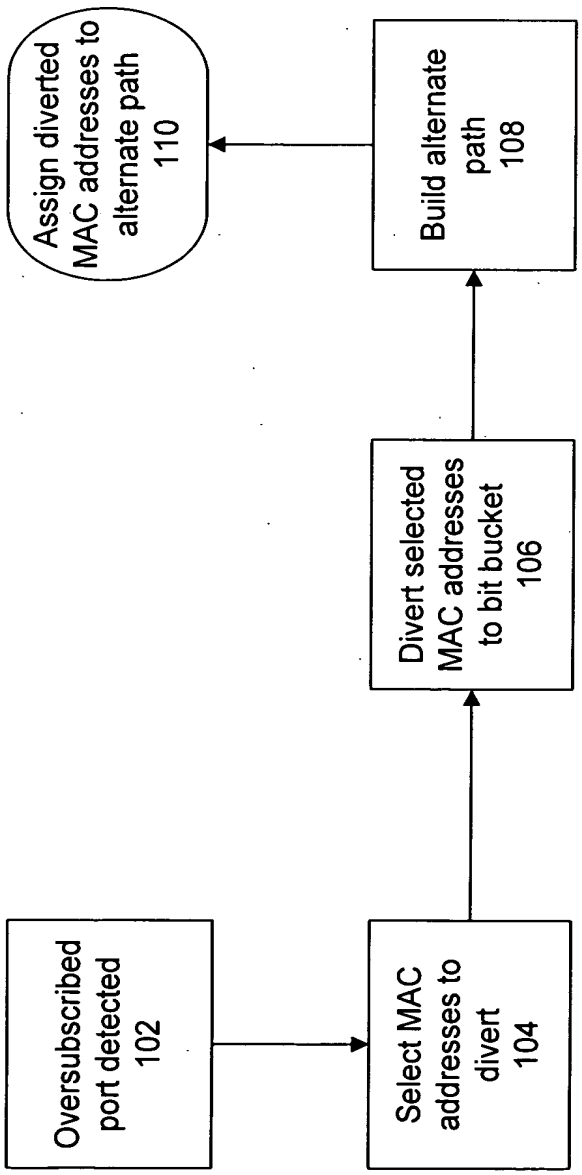


FIG. 1
(Background Art)

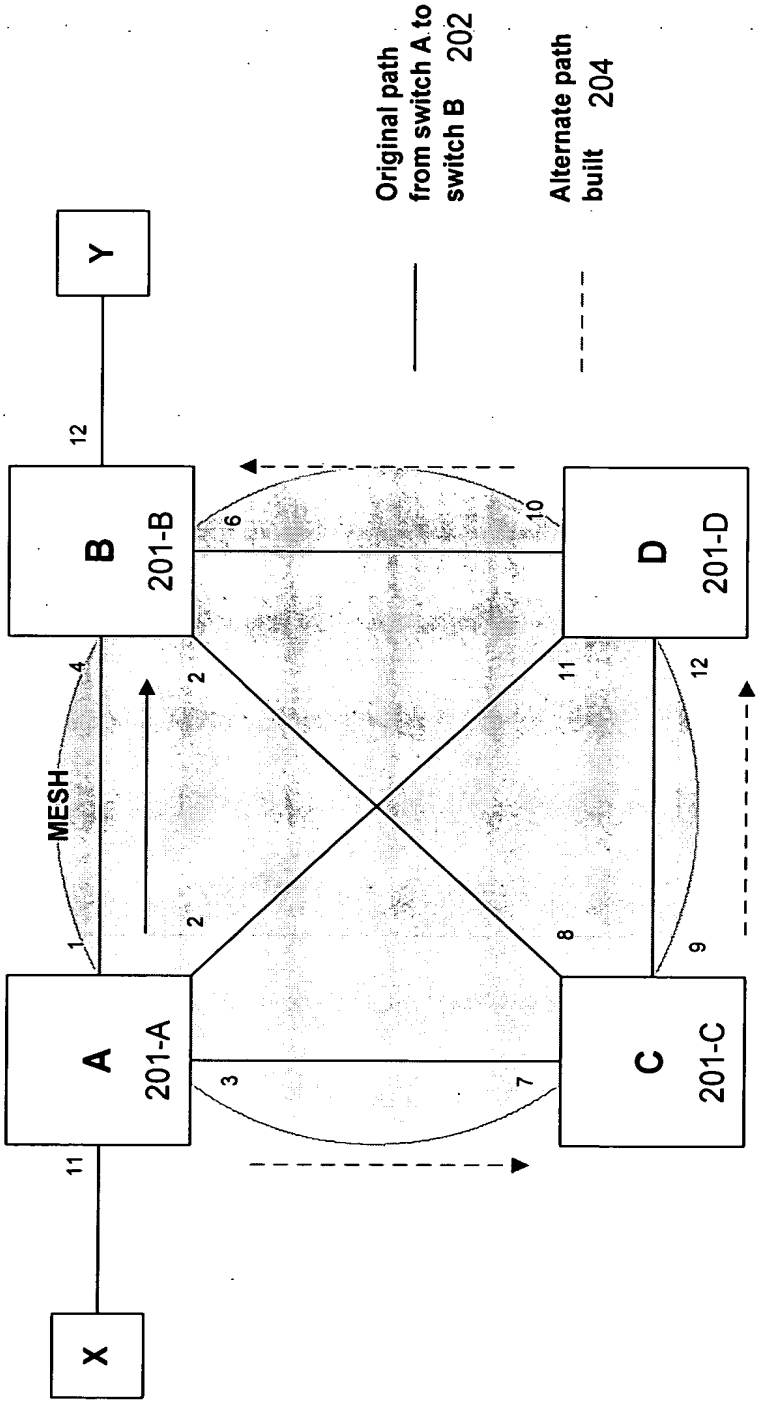


FIG. 2
(Background Art)

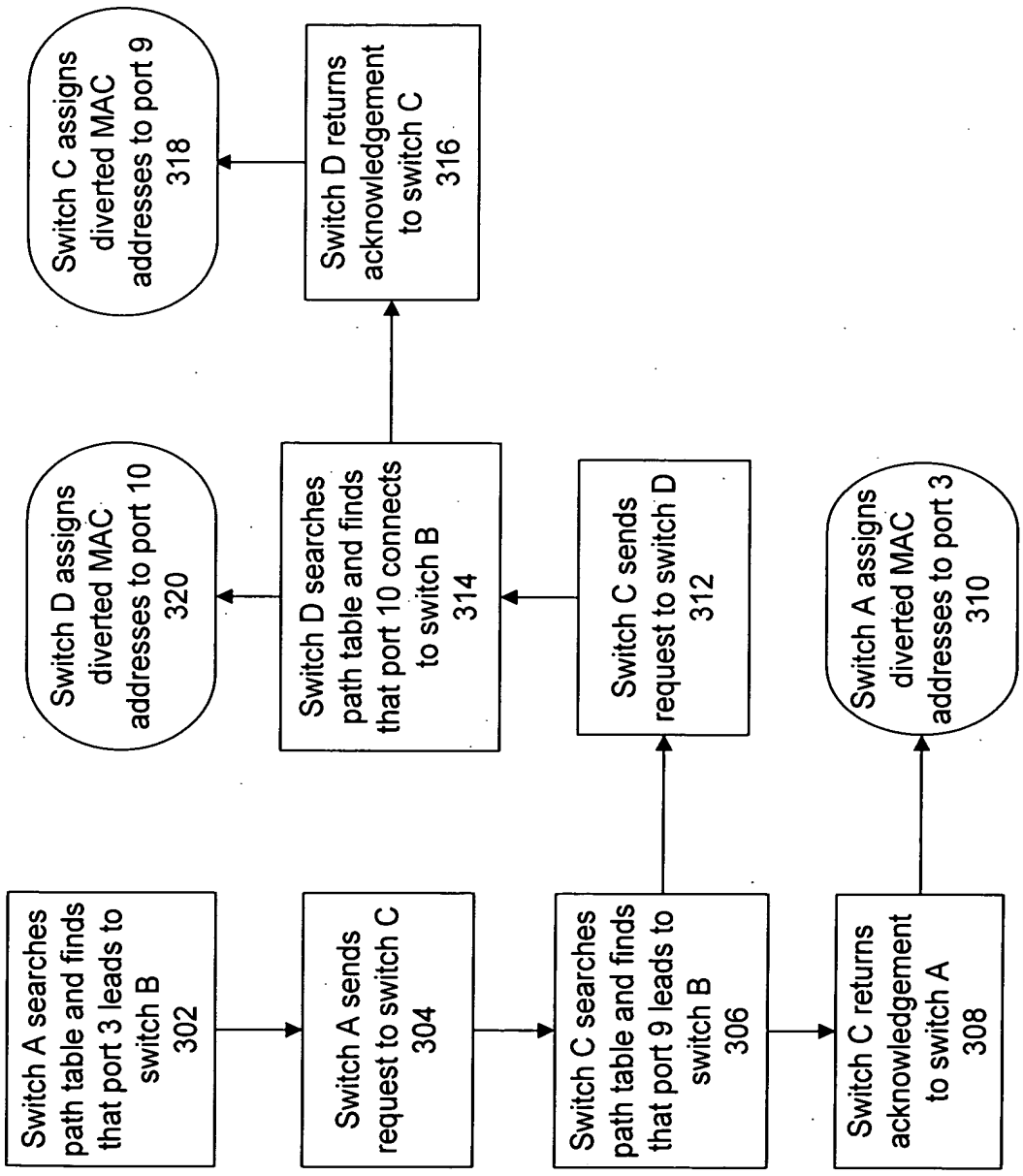


FIG. 3
(Background Art)

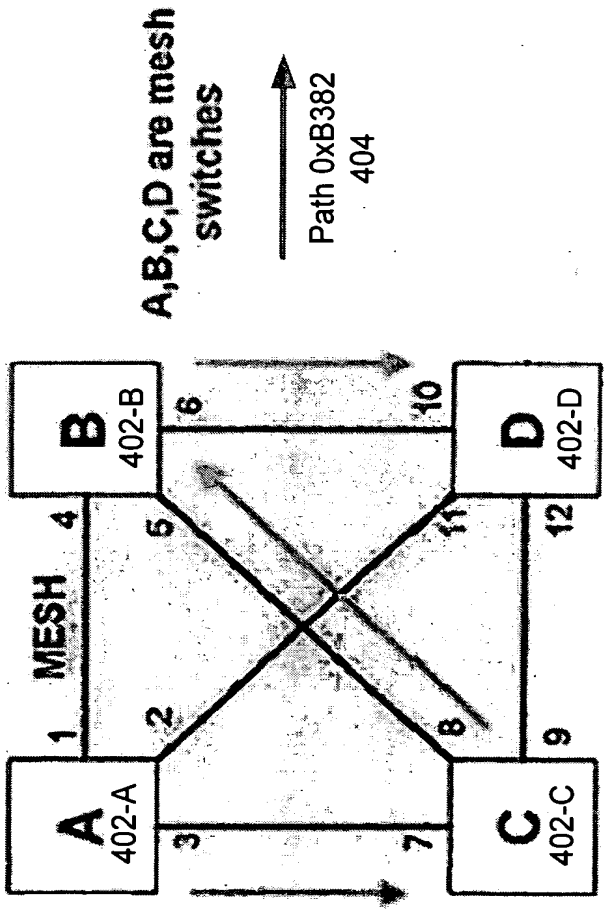

A,B,C,D are mesh switches
Path 0xB382
404
MESH
A
402-A
B
402-B
C
402-C
D
402-D
1
2
3
4
5
6
7
8
9
10
11
12

FIG. 4

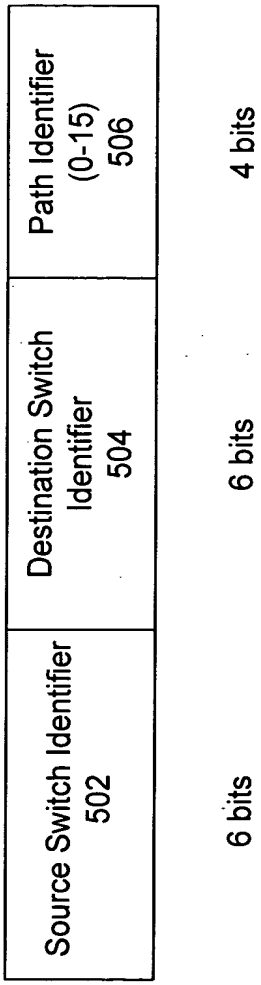

Source Switch Identifier
502
Destination Switch Identifier
504
Path Identifier
(0-15)
506
6 bits
6 bits
4 bits

FIG. 5

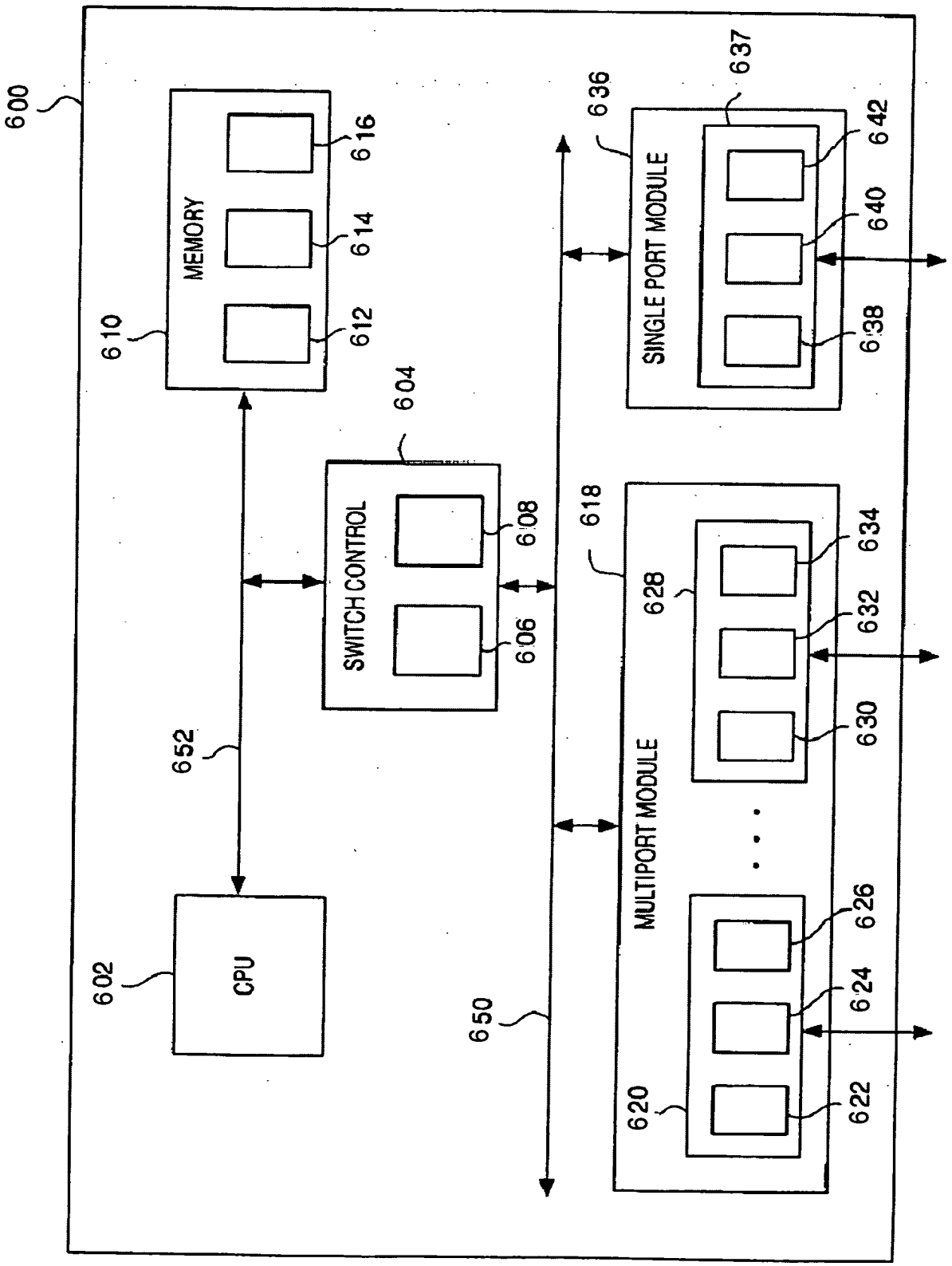
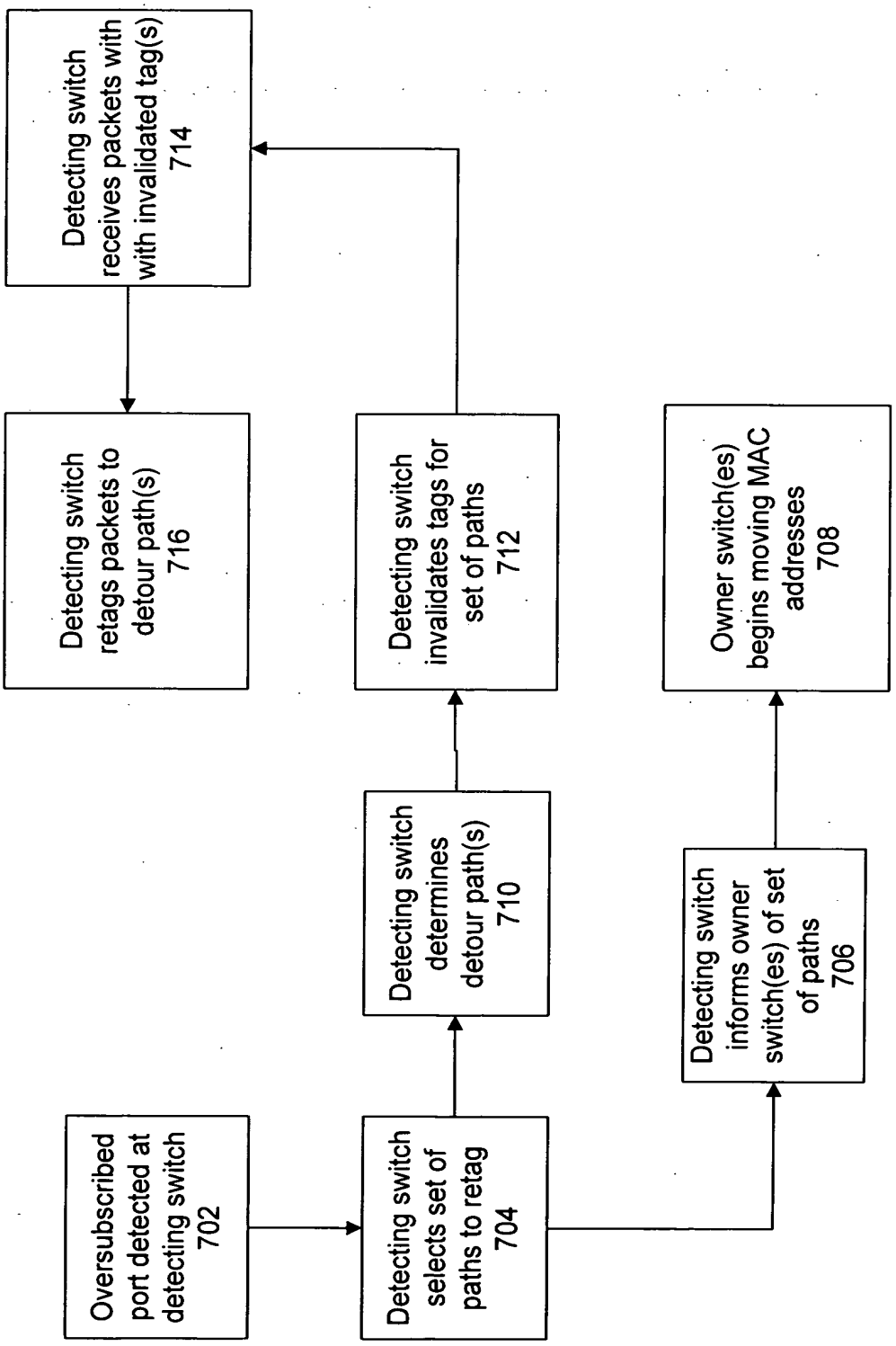

600
MEMORY
610
616
614
612
604
SWITCH CONTROL
608
606
652
CPU
602
650
636
SINGLE PORT MODULE
637
642
640
638
618
MULTIPORT MODULE
628
634
632
630
620
626
624
622

FIG. 6


Oversubscribed port detected at detecting switch 702
Detecting switch selects set of paths to retag 704
Detecting switch informs owner switch(es) of set of paths 706
Detecting switch determines detour path(s) 710
Owner switch(es) begins moving MAC addresses 708
Detecting switch invalidates tags for set of paths 712
Detecting switch receives packets with with invalidated tag(s) 714
Detecting switch retags packets to detour path(s) 716

700

FIG. 7

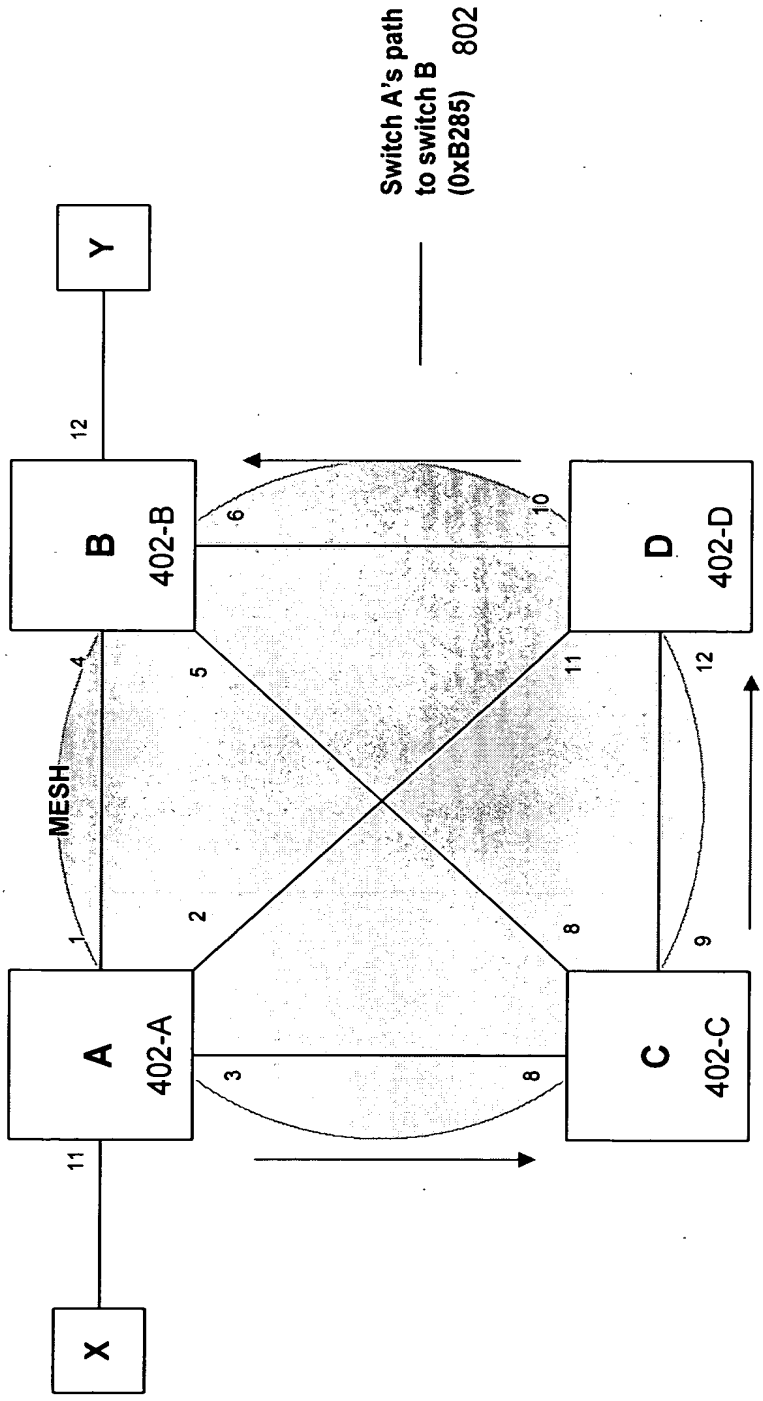

Switch A's path
to switch B
(0xB285) 802
Y
X
A
402-A
B
402-B
C
402-C
D
402-D
MESH
1
2
3
4
5
6
8
9
10
11
12

FIG. 8A

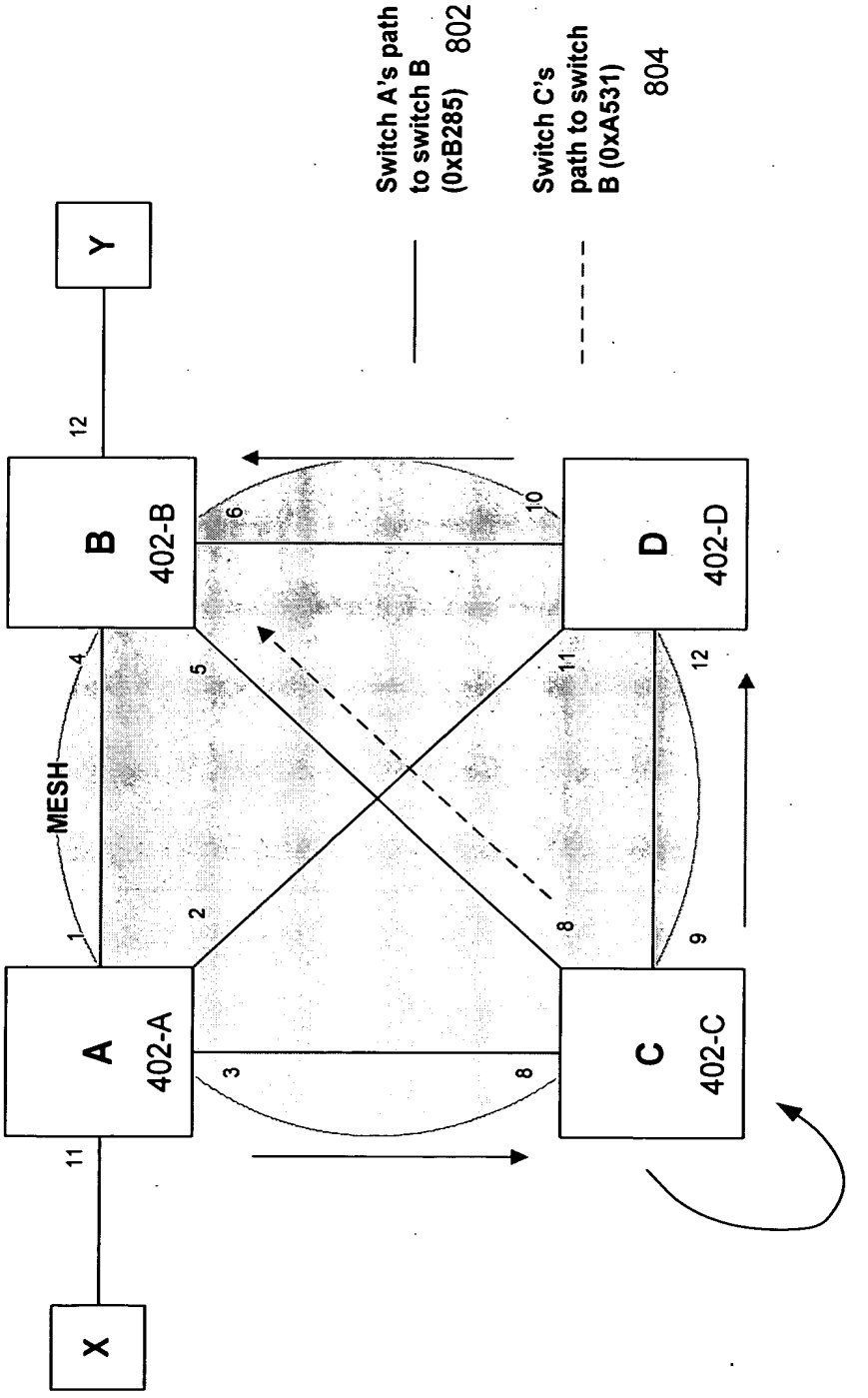

Switch A's path to switch B (0xB285) 802
Switch C's path to switch B (0xA531) 804
Y
X
A 402-A
B 402-B
C 402-C
D 402-D
MESH
Retag 0xB285 to 0xA531
716

FIG. 8B